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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,779	12/09/2003	Feng Lin	DB000861-003	4969

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EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 06/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,779	LIN, FENG	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-5 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-5 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 5 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baker et al. [hereinafter as Baker] [cited by applicant in IDS paper filed on 02/19/04], US Patent 6,445,231 and further in view of Andresen, US Patent 5,808,478 [cited by applicant in IDS paper filed on 02/19/04].

4. As to claim 1, Baker discloses a memory device [100] [col. 3, line 8] comprising: a plurality of memory cells [1 – N, memory banks]; circuits [fig.1], clocked by a local clock [210, CLKout], for writing information into and reading information out of memory cells [col. 3, lines 23 – 30]; and dual-loop for locking said local clock [210] to and an external reference clock signal [208, CLKin] [DLL design [fig. 2A] with a first locked loop [205a, COARSE LOOP] for establishing a first phase relationship between an output signal [CLKout] and a reference signal [CLKin]; and a second locked loop [205b, FINE LOOP] responsive to the first locked loop [205a] and comprising a delay line [DELAY LINE, fig. 12] generating an output signal [CLKout][fig. 11 – 12, and 14]; a control circuit [908, shift register] for controlling the delay of said delay line [col. 8, lines 27 - 30]; a phase detector [902] for producing signals [SL, SR] for input to the control circuit [908] [col. 8, lines 27 – 33, fig. 9]; and a feedback path [1112 – 1110]

for connecting an output [1112] of said delay line to an input [1110] of said first locked loop [11102, coarse loop] [fig. 11] and said phase detector [902], said local clock signal [CLKout] being available at said output [212] of said delay line [col. 8, lines 60 – 65].

However, Baker does not disclose a delay line of second locked loop having a first portion providing a variable amount of delay substantially independent of process, temperature, and voltage [PVT] variation and the second portion in series with the first portion and providing a variable amount of delay that substantially tracks changes in process, temperature and voltage variation. In summary, Backer does not teach chain of delay circuits wherein the first is independent of PVT variation and the second is dependent on PVT variation.

Andresen teaches a system and method for a digitally controlled output buffer with an interleaved delay line with a first portion [40, variable delay] providing a variable amount of delay substantially independent of [does not vary with] process, temperature, and voltage variations [col. 3, lines 59 – 62]; and a second portion [38, intrinsic delay] in series with said first portion and providing a variable amount of delay that substantially tracks [operable to account for] changes [variations] in process, temperature, and voltage [PVT] variations [col. 3, lines 26 - 29, fig. 2]. Andersen discloses to provide a compensated delay between an input and output of logic transition [col. 2, lines 1 – 9], and to vary drive as a function of load such that the slew rate can be made capacitive load independent [col. 2, lines 29 – 34], and also drive level varied without the use of current sources to vary the drive provided to the load [col. 2, lines 34 – 37, col. 3, lines 40 – 45].

It would have been an obvious to one of ordinary skill in art, having the teachings of Baker with Andersen before him at the time of invention was made, to modify the delay line of

second locked loop disclosed by Baker to include a delay line with a first portion [40, variable delay] providing a variable amount of delay substantially independent of [does not vary with] process, temperature, and voltage variations [col. 3, lines 59 – 62]; and a second portion [38, intrinsic delay] in series with said first portion and providing a variable amount of delay that substantially tracks [operable to account for] changes [variations] in process, temperature, and voltage [PVT] variations will effectively vary slew rate such that, when capacitive load is increased, a lower impedance is presented to drive more current into load and, when capacitive load is decreased, the driving impedance is increased to drive less current into load [col. 3, lines 40 – 45].

5. As to claim 2, Baker discloses a memory device [100] [col. 3, line 8] comprising: a plurality of memory cells [1 – N, memory banks]; circuits [fig.1], clocked by a local clock [210, CLKout], for writing information into and reading information out of memory cells [col. 3, lines 23 – 30]; and dual-loop for locking said local clock [210] to and an external reference clock signal [208, CLKin] [DLL design [fig. 2A] with a first locked loop [205a, COARSE LOOP] for establishing a first phase relationship between an output signal [CLKout] and a reference signal [CLKin]; and a second locked loop [205b, FINE LOOP] responsive to the first locked loop [205a] and comprising a delay line [DELAY LINE, fig. 12] generating an output signal [CLKout][fig. 11 – 12, and 14]; a control circuit [908, shift register] for controlling the delay of said delay line [col. 8, lines 27 - 30]; a phase detector [902] for producing signals [SL, SR] for input to the control circuit [908] [col. 8, lines 27 – 33, fig. 9]; and a feedback path [1112 – 1110] for connecting an output [1112] of said delay line to an input [1110] of said first locked loop

[11102, coarse loop] [fig. 11] and said phase detector [902], said local clock signal [CLKout] being available at said output [212] of said delay line [col. 8, lines 60 – 65].

However, Baker does not disclose about a delay line having a first portion with a smaller intrinsic delay, and second portion with larger intrinsic value and producing control signals to control the delay. In summary, Backer does not teach chain of delay with a first portion with smaller and, a second portion with larger intrinsic delay value and producing control signals to control the delay.

Andresen teaches system and method for digitally controlled output buffer with interleaved delay line with a first portion [112] providing a variable amount of delay with little intrinsic delay; a second portion [114] providing a variable amount of delay with larger intrinsic delay [fig. 5, 6], and generating control signal to control the delays of both portions [col. 3, lines 24 – 36, and 58 – 62]. Andersen discloses to provide a compensated delay between an input and output of logic transition [col. 2, lines 1 – 9], and to vary drive as a function of load such that the slew rate can be made capacitive load independent [col. 2, lines 29 – 34], and also drive level varied without the use of current sources to vary the drive provided to the load [col. 2, lines 34 – 37, col. 3, lines 40 – 45].

It would have been an obvious to one of an ordinary skill in art, having the teachings of Baker with Andersen before him at the time of invention was made, to modify the delay line of second locked loop disclosed by Baker to include with a first portion [112] providing a variable amount of delay with little intrinsic delay; a second portion [114] providing a variable amount of delay with larger intrinsic delay [fig. 5, 6] will effectively vary slew rate such that, when capacitive load is increased, a lower impedance is presented to drive more current into load and,

when capacitive load is decreased, the driving impedance is increased to drive less current into load [col. 3, lines 41 – 45].

6. Claims 3 – 5, are rejected under 35 U.S.C. 103(a) as being unpatentable over Baker et al. [hereinafter as Baker] [cited by applicant in IDS paper filed on 02/19/04], US Patent 6,445,231 and further in view of Ono, US Patent 5,923,715.

7. As to claim 3, Baker discloses a memory device [100] [col. 3, line 8] comprising: a plurality of memory cells [1 – N, memory banks]; circuits [fig.1], clocked by a local clock [210, CLKout], for writing information into and reading information out of memory cells [col. 3, lines 23 – 30]; and dual-loop for locking said local clock [210] to and an external reference clock signal [208, CLKin] [DLL design [fig. 2A] with a first locked loop [205a, COARSE LOOP] for establishing a first phase relationship between an output signal [CLKout] and a reference signal [CLKin]; and a second locked loop [205b, FINE LOOP] responsive to the first locked loop [205a] and comprising a delay line [DELAY LINE, fig. 12] generating an output signal [CLKout][fig. 11 – 12, and 14]; a control circuit [908, shift register] for controlling the delay of said delay line [col. 8, lines 27 - 30]; a phase detector [902] for producing signals [SL, SR] for input to the control circuit [908] [col. 8, lines 27 – 33, fig. 9]; and a feedback path [1112 – 1110] for connecting an output [1112] of said delay line to an input [1110] of said first locked loop [11102, coarse loop] [fig. 11] and said phase detector [902], said local clock signal [CLKout] being available at said output [212] of said delay line [col. 8, lines 60 – 65].

However, Baker does not disclose about a delay line of second lock loop having a first circuit path having a stepwise variable capacitive load, and second circuit path in series with first circuit path and having a plurality of stages each having at least two paths and control circuit for

controlling the amount of capacitance in first circuit path and number of stages in second circuit path.

Ono teaches locked loop [digital phase-locked loop] a first locked loop [DLL with phase comparator] to establish a phase relationship [inherent to phase comparator] between an output [F2, DPLL output clock signal] and reference signal [F1, reference clock signal][fig. 1]; a second locked loop [DLL with frequency comparator] responsive to said first locked loop [DLL with phase comparator] [fig.1] and comprising: a delay line [16, variable delay circuit] having a first circuit path [via load cap. Control 12, fig. 1, 2] having a stepwise variable [adder/subtracter circuit increments or decrements] capacitive load [load capacitance] [col. 4, lines 11 – 21]; a second circuit path [via delay stage control 13, fig. 1, 2] having a plurality of stages [number of delay stages] each having at least two paths [with selection of different number of inverters] [col. 4, lines 19 – 24, and lines 48 – 67, col. 5, lines 1 – 14, fig.2]; a control circuit [15, 13, load cap. Control, delay stage control] for controlling the amount of capacitance [load capacitance] in the first circuit path and number of stages [number of delay stages] in the second circuit path [col. 4, lines 48 – 67, col. 5, lines 1 – 14]; a phase detector [14, phase comparator] for producing signals for input to said control circuit [15] [col. 4, lines 8 – 13, fig. 1]; and a feedback path [F2] between an output [Digital PLL output] of second circuit path and an input of the first circuit path and to said phase detector [14][fig.1, 7] which provides small jitter and high accuracy without requiring complicated control algorithm [col. 1, lines 5 – 8].

It would have been an obvious to one of an ordinary skill in art, having the teachings of Baker and Ono before him at the time of invention was made, to modify the delay line of second locked loop disclosed by Baker to include a delay line [16, variable delay circuit] having a first

circuit path [via load cap. Control 12, fig. 1, 2] having a stepwise variable [adder/subtracter circuit increments or decrements] capacitive load [load capacitance] [col. 4, lines 11 – 21]; a second circuit path [via delay stage control 13, fig. 1, 2] having a plurality of stages [number of delay stages] each having at least two paths [with selection of different number of inverters] [col. 4, lines 19 – 24, and lines 48 – 67, col. 5, lines 1 – 14, fig.2]; a control circuit [15, 13, load cap. Control, delay stage control] for controlling the amount of capacitance [load capacitance] in the first circuit path and number of stages [number of delay stages] in the second circuit path [col. 4, lines 48 – 67, col. 5, lines 1 – 14]; a phase detector [14, phase comparator] for producing signals for input to said control circuit [15] [col. 4, lines 8 – 13, fig. 1] to provides small jitter and high accuracy without requiring complicated control algorithm [col. 1, lines 5 – 8].

8. As to claim 4, Baker discloses a memory device [100] [col. 3, line 8] comprising: a plurality of memory cells [1 – N, memory banks]; circuits [fig.1], clocked by a local clock [210, CLKout], for writing information into and reading information out of memory cells [col. 3, lines 23 – 30]; and dual-loop for locking said local clock [210] to and an external reference clock signal [208, CLKin] [DLL design [fig. 2A] with a first locked loop [205a, COARSE LOOP] for establishing a first phase relationship between an output signal [CLKout] and a reference signal [CLKin]; and a second locked loop [205b, FINE LOOP] responsive to the first locked loop [205a] and comprising a delay line [DELAY LINE, fig. 12] generating an output signal [CLKout][fig. 11 – 12, and 14]; a control circuit [908, shift register] for controlling the delay of said delay line [col. 8, lines 27 - 30]; a phase detector [902] for producing signals [SL, SR] for input to the control circuit [908] [col. 8, lines 27 – 33, fig. 9]; and a feedback path [1112 – 1110] for connecting an output [1112] of said delay line to an input [1110] of said first locked loop

[11102, coarse loop] [fig. 11] and said phase detector [902], said local clock signal [CLKout] being available at said output [212] of said delay line [col. 8, lines 60 – 65].

However, Baker does not disclose about a delay line of second lock loop having a first circuit path having a stepwise variable capacitive load, and second circuit path in series with first circuit path and having a plurality of stages each having a variable amount of drive associated therewith and control circuit for controlling the amount of capacitance in first circuit path and number of stages in second circuit path.

Ono teaches locked loop [digital phase-locked loop], a first locked loop [DLL with phase comparator] to establish a phase relationship [inherent to phase comparator] between an output [F2, DPLL output clock signal] and reference signal [F1, reference clock signal][fig. 1]; a second locked loop [DLL with frequency comparator] responsive to said first locked loop [DLL with phase comparator] [fig.1] and comprising: a first circuit path [via load cap. Control 12, fig. 1, 2] having a stepwise variable [adder/subtracter circuit increments or decrements] capacitive load [load capacitance] [col. 4, lines 11 – 21]; a second circuit path [via delay stage control 13, fig. 1, 2] having a plurality of stages [number of delay stages] each having at least two paths [with selection of different number of inverters] [col. 4, lines 19 – 24, and lines 48 – 67, col. 5, lines 1 – 14, fig.2]; a control circuit [15, 13, load cap. Control, delay stage control] for controlling the amount of capacitance [load capacitance] in the first circuit path and number of stages [number of delay stages] in the second circuit path [col. 4, lines 48 – 67, col. 5, lines 1 – 14]; a phase detector [14, phase comparator] for producing signals for input to said control circuit [15] [col. 4, lines 8 – 13, fig. 1]; and a feedback path [F2] between an output [Digital PLL output] of second circuit path and an input of the first circuit path and to said phase detector [14][fig.1, 7], which

provides small jitter and high accuracy without requiring complicated control algorithm [col. 1, lines 5 – 8].

It would have been an obvious to one of an ordinary skill in art, having the teachings of Baker and Ono before him at the time of invention was made, to modify the delay line of second locked loop disclosed by Baker to include a delay line [16, variable delay circuit] having a first circuit path [via load cap. Control 12, fig. 1, 2] having a stepwise variable [adder/subtracter circuit increments or decrements] capacitive load [load capacitance] [col. 4, lines 11 – 21]; a second circuit path [via delay stage control 13, fig. 1, 2] having a plurality of stages [number of delay stages] each having at least two paths [with selection of different number of inverters] [col. 4, lines 19 – 24, and lines 48 – 67, col. 5, lines 1 – 14, fig.2]; a control circuit [15, 13, load cap. Control, delay stage control] for controlling the amount of capacitance [load capacitance] in the first circuit path and number of stages [number of delay stages] in the second circuit path [col. 4, lines 48 – 67, col. 5, lines 1 – 14]; a phase detector [14, phase comparator] for producing signals for input to said control circuit [15] [col. 4, lines 8 – 13, fig. 1]; and a feedback path [F2] between an output [Digital PLL output] of second circuit path and an input of the first circuit path and to said phase detector [14][fig.1, 7] to provide small jitter and high accuracy without requiring complicated control algorithm [col. 1, lines 5 – 8].

9. As to claim 5, Baker discloses a memory device [100] [col. 3, line 8] comprising: a plurality of memory cells [1 – N, memory banks]; circuits [fig.1], clocked by a local clock [210, CLKout], for writing information into and reading information out of memory cells [col. 3, lines 23 – 30]; and dual-loop for locking said local clock [210] to and an external reference clock signal [208, CLKin] [DLL design [fig. 2A] with a first locked loop [205a, COARSE LOOP] for

establishing a first phase relationship between an output signal [CLKout] and a reference signal [CLKin]; and a second locked loop [205b, FINE LOOP] responsive to the first locked loop [205a] and comprising a delay line [DELAY LINE, fig. 12] generating an output signal [CLKout][fig. 11 – 12, and 14]; a control circuit [908, shift register] for controlling the delay of said delay line [col. 8, lines 27 - 30]; a phase detector [902] for producing signals [SL, SR] for input to the control circuit [908] [col. 8, lines 27 – 33, fig. 9]; and a feedback path [1112 – 1110] for connecting an output [1112] of said delay line to an input [1110] of said first locked loop [11102, coarse loop] [fig. 11] and said phase detector [902], said local clock signal [CLKout] being available at said output [212] of said delay line [col. 8, lines 60 – 65].

However, Baker does not disclose a delay line of second locked loop having a first circuit path having a plurality of stages each having a variable amount of drive associated therewith and second circuit path having a plurality of stages each having at least a fast and slow path, and control circuit for controlling the number of stages in first circuit path and the number of stages in the second circuit path.

Ono teaches locked loop [digital phase-locked loop], a first locked loop [DLL with phase comparator] to establish a phase relationship [inherent to phase comparator] between an output [F2, DPLL output clock signal] and reference signal [F1, reference clock signal][fig. 1]; a second locked loop [DLL with frequency comparator] responsive to said first locked loop [DLL with phase comparator] [fig.1] and comprising: a first circuit path [via load cap. Control 12, fig. 1, 2] having a variable amount [adder/subtracter circuit increments or decrements] of drive [load capacitance] associated therewith [col. 4, lines 11 – 21]; a second circuit path [via delay stage control 13, fig. 1, 2] having a plurality of stages [number of delay stages] each having at least a

fast [with less number of delay stages] and slow [with more number of delay stages] path [with selection of different number of inverters] [col. 4, lines 19 – 24, and lines 48 – 67, col. 5, lines 1 – 14, fig.2]; a control circuit [15, 13, load cap. Control, delay stage control] for controlling number of stages [number of capacitive load stages] in the first circuit path and number of stages [number of delay stages] in the second circuit path [col. 4, lines 48 – 67, col. 5, lines 1 – 14]; a phase detector [14, phase comparator] for producing signals for input to said control circuit [15] [col. 4, lines 8 – 13, fig. 1]; and a feedback path [F2] between an output [Digital PLL output] of second circuit path and an input of the first circuit path and to said phase detector [14][fig.1, 7], which provides small jitter and high accuracy without requiring complicated control algorithm [col. 1, lines 5 – 8].

It would have been an obvious to one of an ordinary skill in art, having the teachings of Baker and Ono before him at the time of invention was made, to modify the delay line of second locked loop disclosed by Baker to include a delay line [16, variable delay circuit] having a first circuit path [via load cap. Control 12, fig. 1, 2] having a variable amount [adder/subtracter circuit increments or decrements] of drive [load capacitance] associated therewith [col. 4, lines 11 – 21]; a second circuit path [via delay stage control 13, fig. 1, 2] having a plurality of stages [number of delay stages] each having at least a fast [with less number of delay stages] and slow [with more number of delay stages] path [with selection of different number of inverters] [col. 4, lines 19 – 24, and lines 48 – 67, col. 5, lines 1 – 14, fig.2]; a control circuit [15, 13, load cap. Control, delay stage control] for controlling number of stages [number of capacitive load stages] in the first circuit path and number of stages [number of delay stages] in the second circuit path [col. 4, lines 48 – 67, col. 5, lines 1 – 14]; a phase detector [14, phase comparator] for producing signals for

input to said control circuit [15] [col. 4, lines 8 – 13, fig. 1]; and a feedback path [F2] between an output [Digital PLL output] of second circuit path and an input of the first circuit path and to said phase detector [14][fig.1, 7], which provides small jitter and high accuracy without requiring complicated control algorithm [col. 1, lines 5 – 8] to provide small jitter and high accuracy without requiring complicated control algorithm [col. 1, lines 5 – 8].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 703-305-3994. The examiner can normally be reached on 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Brown can be reached on 703-308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
June 23, 2004

LYNNE H. BROWNE
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TECHNOLOGY CENTER ~~2600~~ 2100